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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,364	08/21/2003	Gilles Amblard	H1902 / AMDP981US	7431

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EXAMINER	
CHACKO DAVIS, DABORAH	

ART UNIT	PAPER NUMBER
1756	

NOTIFICATION DATE	DELIVERY MODE
09/12/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/645,364	AMBLARD ET AL.	
	Examiner	Art Unit	
	Daborah Chacko-Davis	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-8, 10, and 17-24, are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent No. 6,650,422 (Singh et al, hereinafter referred to as Singh) in view of U. S. Patent No. 6,6561,706 (Singh et al, herein after referred to as Singh '706) and U. S. Patent No. 6,905,949 (Arita).

Singh, in the abstract, in col 1, lines 32-39, in col 2, lines 14-52, in col 3, lines 8-20, in col 4, lines 1-12, in col 6, lines 6-66, in col 9, lines 1-15, and lines 45-67, discloses a method for selectively mitigating asymmetry in the pattern profile of features (line widths, spacing, packing density, surface geometry) on a semiconductor device, using scatterometry techniques (using scatterometry system), and detectors that characterize and measure data from the photoresist pattern and determine the pattern profile from the collected data, storing the determined profile in the memory component of the processor system, determining the profile characteristics of each side of the photoresist pattern feature by comparing data associated with known feature profiles (means for making inferences related to photoresist line status) , and ascertaining the asymmetry for both sides of the feature. Singh, in col 9, lines 1-15, discloses that the data set associated with the features under analysis may be put into the trained neural

network (artificial intelligence) which will then provide a determination of the state of the feature profile (making inferences), and the asymmetric information associated with the feature under analysis is feedback or fed forward into fabrication process parameters (including repeated exposing, developing and etching processes, removing excess material etc., i.e., the trim etch component) (and generating feedback). Singh, in col 4, lines 59-67, in col 5, lines 1-29, in col 9, lines 1-67, in col 10, lines 1-60, discloses that the features of profile desired (original profile of a feature) is compared to the feature profile data and then the asymmetry is ascertained and feedback or feedforward process control data is generated to correct the asymmetry determined and fabrication process parameters is altered i.e., etch processes or CMP processes are altered in accordance to the asymmetry ascertained i.e., the trim etch component (a final correction) corrects the asymmetry so as to attain the desired original profile on the photoresist features (claims 1, 3-8, 10, and 17-21, 23-24).

The difference between the claims and Singh is that Singh does not disclose that the pattern profiles determined, for mitigation and/or for trimming , on the photoresist features are that of line-edge roughness, and critical dimensions. Singh does not disclose mitigating LER using the non-lithographic technique (claim 22).

Singh '706, in col 2, lines 14-66, in col 5, lines 47-67, discloses a system that monitors the photoresist pattern features and generate information from scatterometric analysis, and control subsequent processes based on the collected data from monitoring previous processes, and therefore facilitate achieving desired critical

dimensions and pattern dimensions (such as width, spacing, slope of the sides of a feature, etc.).

The difference between the claims and Singh in view of Singh '706 is that Singh in view of Singh '706 does not disclose the mitigation of line-edge roughness.

Arita, in col 4, lines 1-9, discloses a non-lithographic shrink component (technique) employed to eliminate the edge roughness of the resist pattern (line-edge roughness).

Therefore, it would be obvious to a skilled artisan to modify Singh by employing the method of monitoring features such as CD and LER as suggested by Singh '706 because Singh '706, in col 2, lines 46-63, and in col 3, lines 1-28, discloses that determining desired critical dimensions and characteristics of patterned features lead to substantial uniformity of critical dimensions between layers, which in turn facilitates higher speeds in such chips. It would be obvious to a skilled artisan to modify Singh in view of Singh '706 by employing the method suggested by Arita to eliminate the edge roughness of the photoresist pattern because the Arita, in col 4, lines 1-9, and in col 5, lines 15-42, discloses that the elimination of the edge roughness (by a non-lithographic component) of the resist pattern in the extending direction i.e., line direction prevents the variation of the linewidth of the resist pattern.

3. Claims 9, 11-16, are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent No. 6,650,422 (Singh et al, hereinafter referred to as Singh) in view of U. S. Patent No. 6,6561,706 (Sing et al, herein after referred to as Singh '706) and U. S.

Patent No. 6,905,949 (Arita) as applied to claims 1-8, 10, and 17-24 above, and further in view of U. S. Patent No. 6,730,458 (Kim et al., hereinafter referred to as Kim).

Singh in view of Sing '706 is discussed in paragraph no. 2.

Singh, in the abstract, in col 2, lines 14-52, in col 3,lines 8-20, in col 4, lines 1-12, in col 6, lines 6-66, in col 9, lines 1-15, and lines 45-49, discloses determining the photoresist pattern profile from the collected data, storing the determined profile in the memory component of the processor system, determining the profile characteristics of each side of the photoresist pattern feature by comparing data associated with known feature profiles, and ascertaining the asymmetry for both sides of the feature. Singh, in col 9, lines 1-15, discloses that the data set associated with the features under analysis may be put into the trained neural network (artificial intelligence) which will then provide a determination of the state of the feature profile (making inferences), and the asymmetric information associated with the feature under analysis is feedback or fed forward into fabrication process parameters (and generating feedback) (claims 11-14, and 16).

The difference between the claims and Singh in view of Singh '706 and Arita is that Singh in view of Singh '706 and Arita does not disclose that the non-lithographic shrink component comprises one of the claimed components recited in claims 9, and 15.

Kim, in col 2, lines 3-16, discloses using RELACS processes (non-lithographic shrink component, a chemical technique) for correcting line-edge roughness.

Therefore, it would be obvious to a skilled artisan to modify Singh in view of Singh '706 by employing RELACS processes suggested by Kim because Kim, in col 2, lines 3-24, discloses that implementing RELACS and thermal flow in photoresist pattern results in the reduction of viscosity of the polymerized photoresist and allows it to flow or slump, thereby reducing of the size of the contact openings to achieve fine patterns of desired contact hole sizing.

Response to Arguments

4. Applicant's arguments filed June 22, 2006, have been fully considered but they are not persuasive. The 103 rejections made in the previous office action are maintained.

A) Applicants argue that none of the references disclose satisfying a critical dimension as a result of a deviation presented during a non-lithographic shrink technique.

Singh (6,650,422) is depended upon to disclose accurately detecting asymmetry in the profile of a feature formed on a wafer (resist pattern, etched pattern etc.), adjusting process parameters that are subsequently performed (processes performed after exposure, and development of the feature) based upon the asymmetry detected; the subsequent processes (such as etching, adjusting post-exposure processes, CMP etc) are performed to compensate for the final asymmetry; whether the asymmetry is formed by any of the number of process (a lot of processes are performed on a resist pattern prior to exposing and after exposing and after developing that are not

lithographic components) that does not include exposing and developing is immaterial because Singh, in col 4, lines 59-67, in col 5, lines 1-28, discloses that the feature formed is detected via a detector and compared to against a database that has data of an original feature profile or a known feature profile and then the asymmetry is ascertained followed by determination of correction processes (subsequent processes or fabrication process) to be performed on the determined final asymmetry i.e., any deviation of the feature profile is corrected by etching or CMP etc. and thus satisfying a desired photoresist feature profile. Singh, in col 6, lines 12-18, and lines 29-31, discloses that the features whose asymmetry are to be determined are that of photoresist features (reference 61a of figure 2). Although Singh does not disclose CD, Singh '706 is depended upon to disclose monitoring the photoresist features to determine photoresist profile features such as critical dimension and pattern profile of the monitored photoresist features. Arita is depended upon to disclose a non-lithographic shrink component to eliminate edge roughness (LER) of the resist pattern.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daborah Chacko-Davis whose telephone number is (571) 272-1380. The examiner can normally be reached on M-F 9:30 - 6:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark F Huff can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

dcd

September 4, 2007.